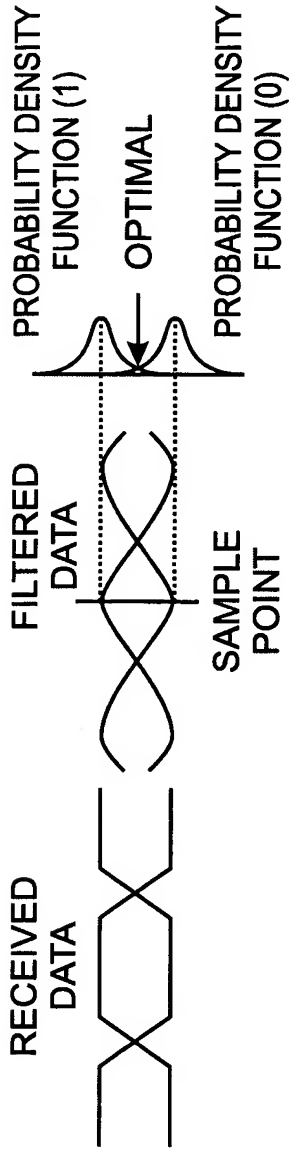

FIG. 1
(Prior Art)

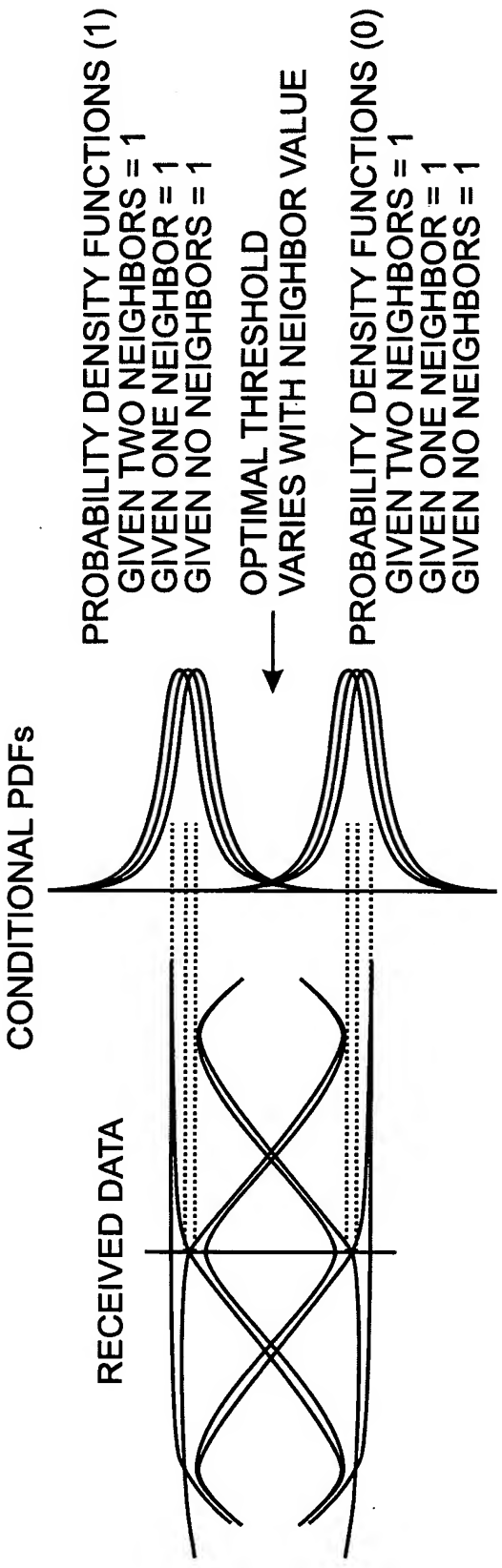

FIG. 2
(Prior Art)

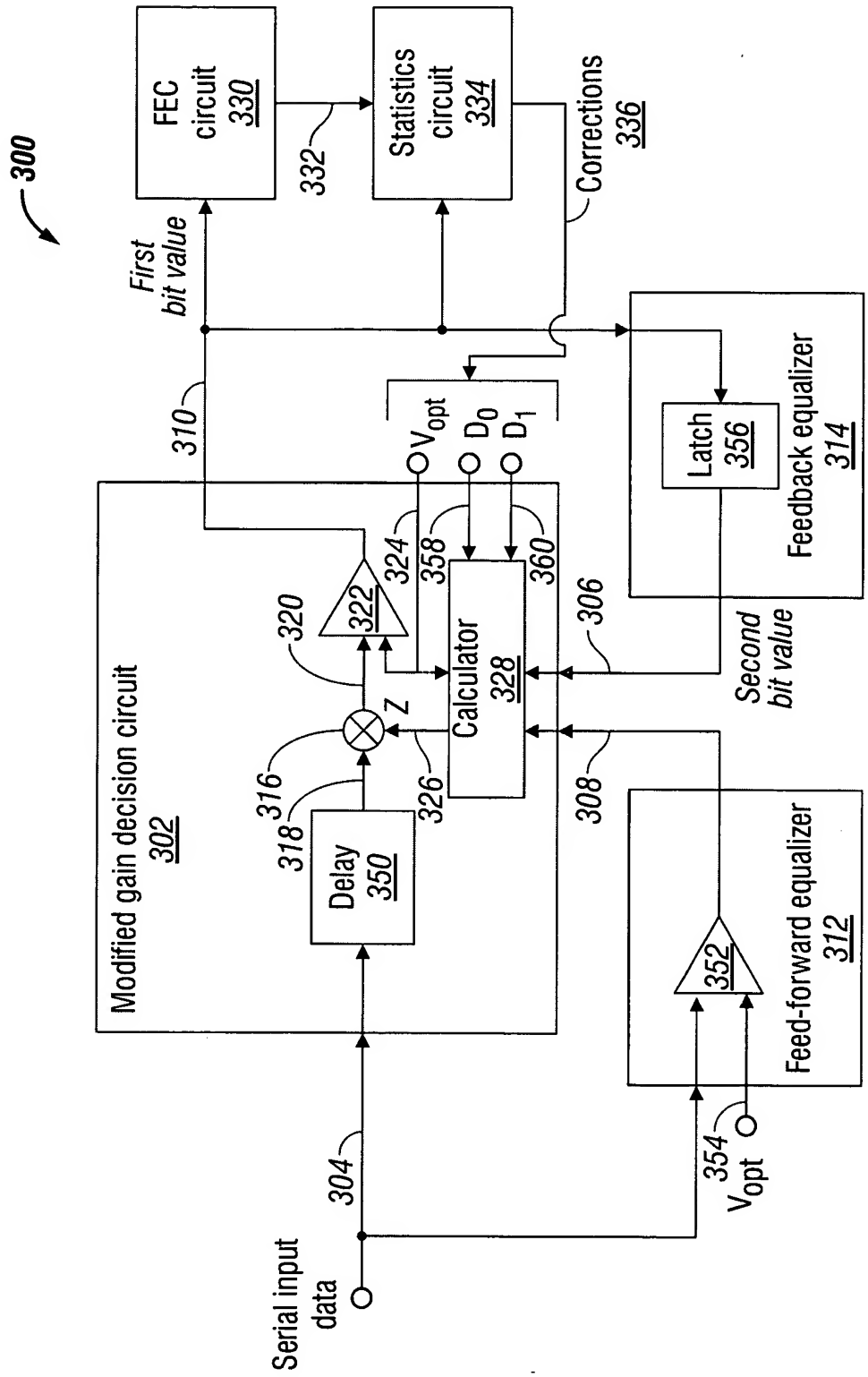
300
FEC circuit 330
332
Statistics circuit 334
Corrections 336
First bit value
310
Modified gain decision circuit 302
V_{opt}
D_0
D_1
Latch 356
Feedback equalizer 314
324
358
360
320
322
306
Calculator 328
Second bit value
Z
316
318
Delay 350
326
308
Feed-forward equalizer 312
352
354
V_{opt}
304
Serial input data

FIG. 3

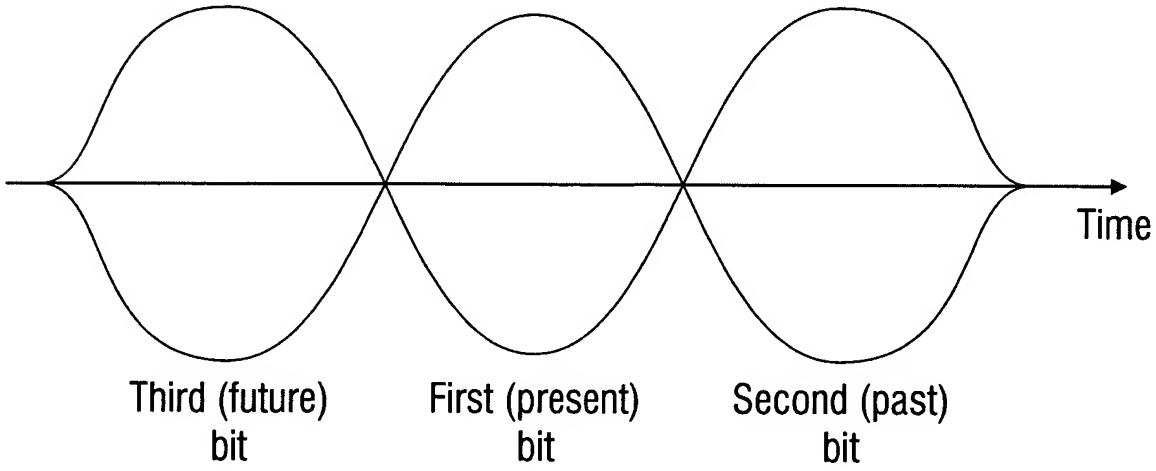
Time
Third (future) bit
First (present) bit
Second (past) bit

FIG. 4

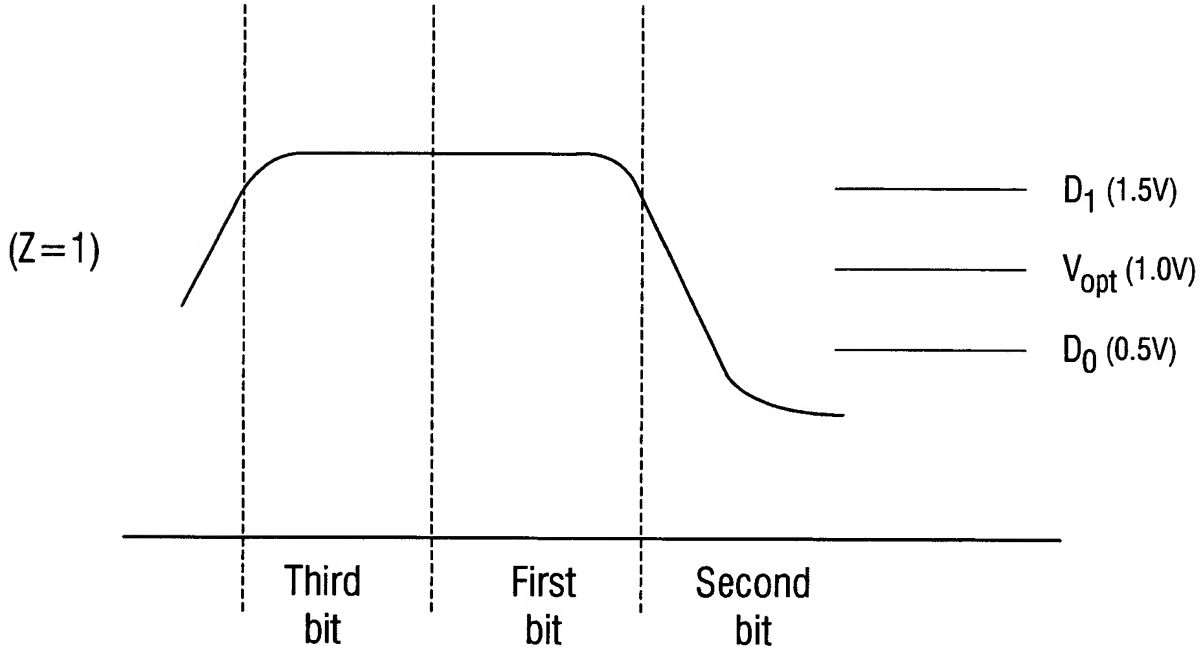
(Z=1)
D_1 (1.5V)
V_{opt} (1.0V)
D_0 (0.5V)
Third bit
First bit
Second bit

FIG. 5

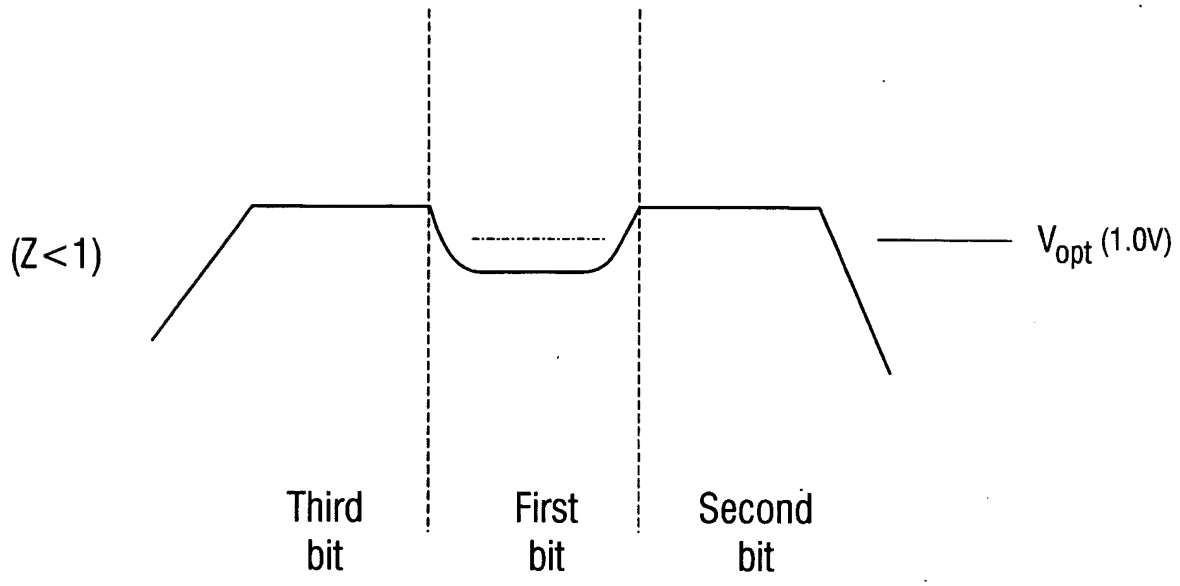

FIG. 6

INPUT LEVEL

D_1	Definite "1"
	"0" If both past and future bit values = "1"
	"1" Otherwise
V_{opt}	
	"1" If both past and future bit values = "0"
	"0" Otherwise
D_0	Definite "0"

FIG. 7

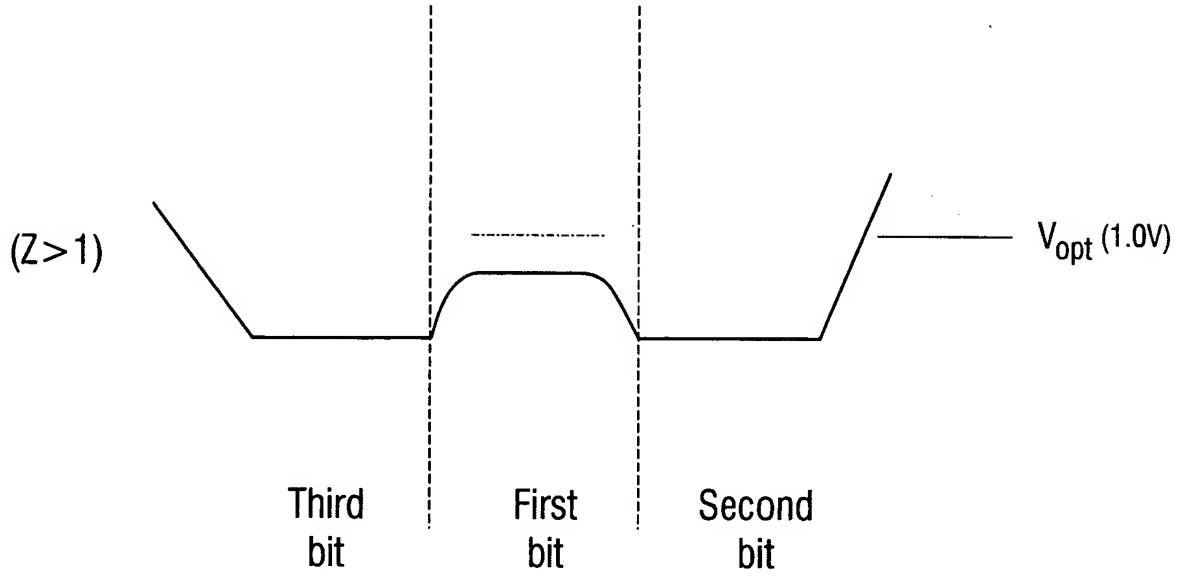

FIG. 8

Amplitude modifier	Second bit value	Third bit value
Low	1	1
High	0	0
Unity	1	0
Unity	0	1

FIG. 9

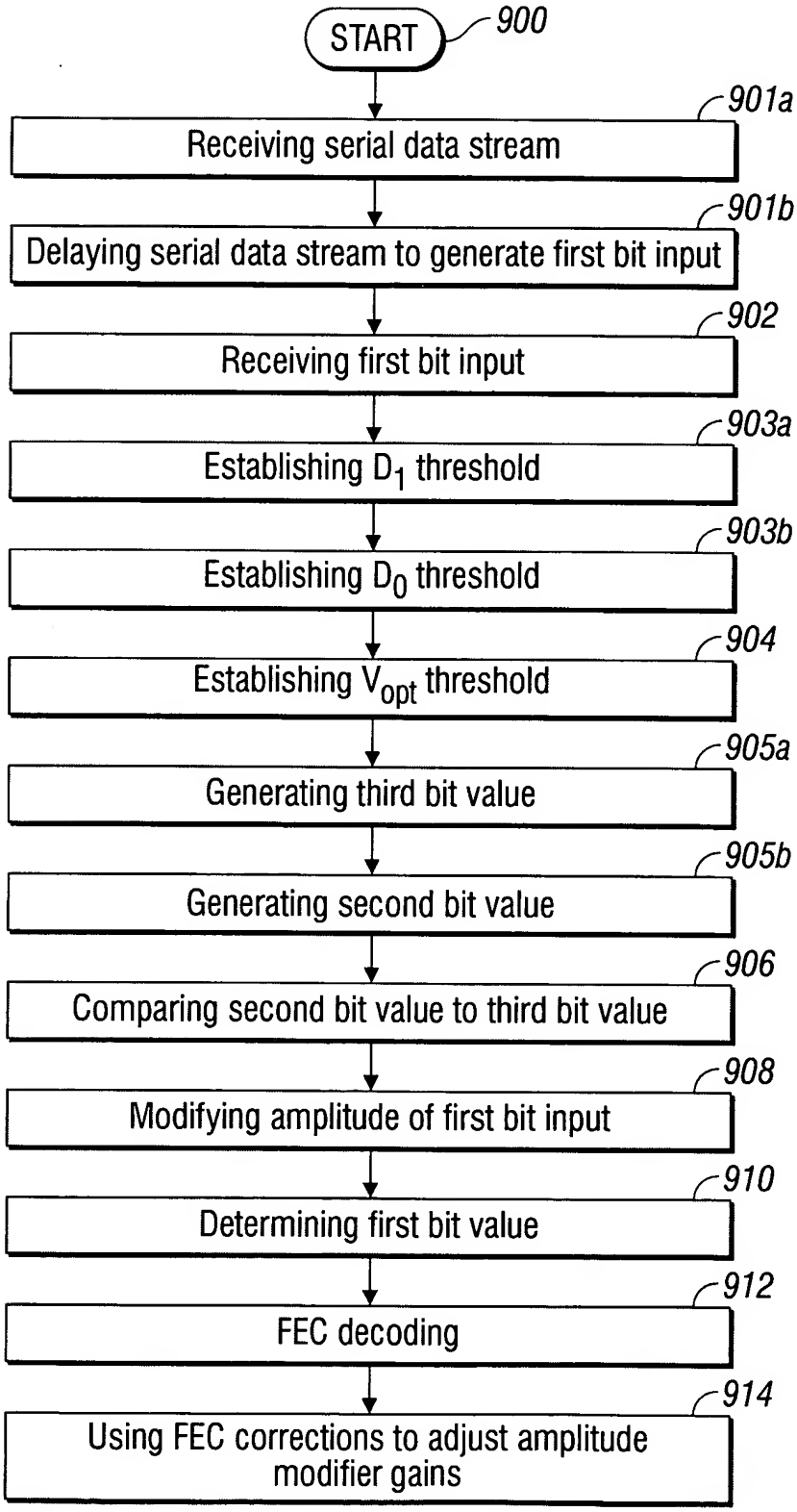
START
900
901a
Receiving serial data stream
901b
Delaying serial data stream to generate first bit input
902
Receiving first bit input
903a
Establishing D_1 threshold
903b
Establishing D_0 threshold
904
Establishing V_{opt} threshold
905a
Generating third bit value
905b
Generating second bit value
906
Comparing second bit value to third bit value
908
Modifying amplitude of first bit input
910
Determining first bit value
912
FEC decoding
914
Using FEC corrections to adjust amplitude modifier gains

FIG. 10